"Power Electronic Building Block design and hardware demonstrator - Results from December 1996 through May 1998"

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Abstract

Results are presented on the US Navy's continuing work in the Power Electronic Building Block (PEBB) program for the period December 1996 through May 1998. The PEBB program, sponsored by the Office of Naval Research, seeks to develop a general purpose power controller capable of performing numerous electrical power conversion functions simply through software reconfiguration. This program is broken into 3 stages. Stage 1 covers PEBB function. Stage 2 covers PEBB form and function. Stage 3 covers PEBB form, fit and function. This paper reports on the Naval Surface Warfare Center Annapolis Detachment efforts in Stage 2 - PEBB form and function. A particular soft switched power conversion topology, the auxiliary resonant commutated pole (ARCP), was developed to demonstrate a PEBB and to test emerging semiconductor devices, namely the p-type and n-type MOS-Controlled Thyristors (MCT) from Harris Semiconductor. Power circuit phase leg design changes and control enhancements relative to the PEBB-1 functional demonstrator will be discussed. Waveform data will be presented and discussed.

ARCP Inverter Development

As a contributor to the Office of Naval Research's (ONR) Power Electronic Building Block (PEBB) program, the Carderock Division, Annapolis Detachment of the Naval Surface Warfare Center (CDNSWC/A) has developed a 250 kW three phase electrical power inverter. Using a combination of MCTs (MOS Controlled Thyristors) and IGBTs (Insulated Gate Bipolar Transistors) manufactured by Harris Semiconductor and employing an ARCP (Auxiliary Resonant Commutated Pole) power switching and control topology, the inverter is being evaluated as a candidate component for use in future US Navy shipboard electrical distribution systems. The ARCP is a soft switching approach that forces the voltage across the main power switch to zero prior to being turned on. This reduces turn on losses of the main load current conducting switch and is projected to improve overall efficiency at high power levels. A detailed description of ARCP operation can be found in reference [1]. MCTs have been developed and provided under the ONR PEBB development program. These devices can withstand high dv/dt and di/dt stresses making them ideal candidates for use as AC auxiliary switches in the ARCP topology. This report summarizes the step by step progress made in the development of the control software used to run the laboratory ARCP inverter.

In the ARCP topology (Figure 1), the voltage is driven to zero across each phase switch (S1 and S2) just prior to its turn on. This is accomplished by generating a resonant current pulse that drives the voltage across the switch to zero. The resonant pulse is formed when an AC switch (A1 and A2) is turned on just prior to turning off a phase switch. When the AC switch is gated on, a current begins to rise linearly through the resonant inductor and the conducting phase switch. When the phase switch is turned off, the current resonates based on the resonant component values and then falls

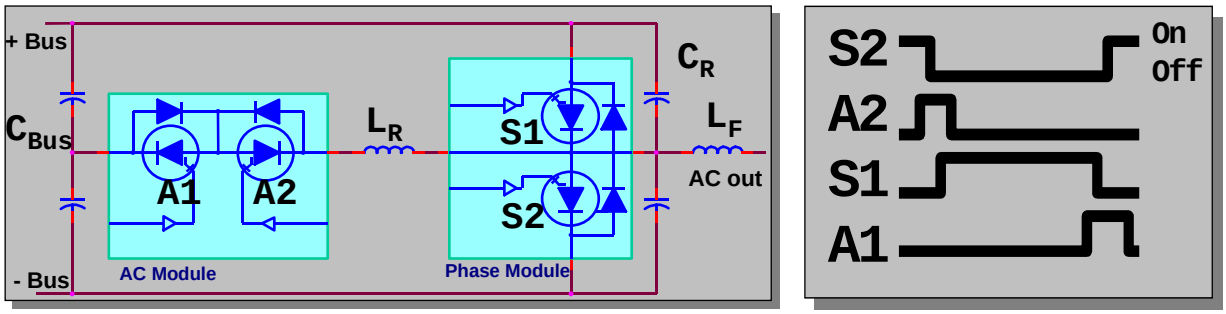

Figure 1. ARCP schematic and switch timing.

back to zero. The peak resonant current depends on the following (see Figure 2):

1. Length of time that both the AC switch and the phase switch are on simultaneously (overlap time)
2. Input bus voltage
3. Resonant component values (L_r and C_r)

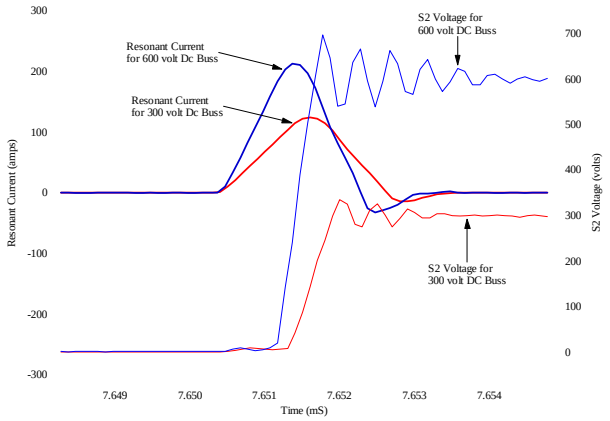

Figure 2. ARCP Resonant Transitions.

The current initially ramps linearly at a rate defined by di/dt = V/(2*L). When the phase switch is turned off, the current continues to rise based on the resonant component values then cycles back to zero. As long as enough energy has been provided in the resonant pulse, the voltage across the opposite phase switch will be driven to zero and it can be turned on. The Harris Semiconductor designed gate drive boards have a zero voltage turn on feature. If a gate signal reaches the board and the voltage across the device has not dropped below 15 volts, the gate drive board will wait until the voltage drops within this range before applying a gate drive signal to the phase switch.

Resonant Pulse Control

Original testing of the ARCP inverter took place with fixed overlap time. This meant that the time between the gating of the AC switch and the turning off of the phase switch could be programmed to a fixed value. Each time a new input DC bus voltage was selected a new fixed overlap time had to be programmed into the controller. Likewise, as load current was increased the fixed overlap time had to be extended to ensure zero voltage was forced on the opposite main switch. This method was quite inefficient because large resonant currents were generated at each switching event Figure 3 displays the high frequency resonant pulses along with the fundamental output load current under fixed overlap operation.

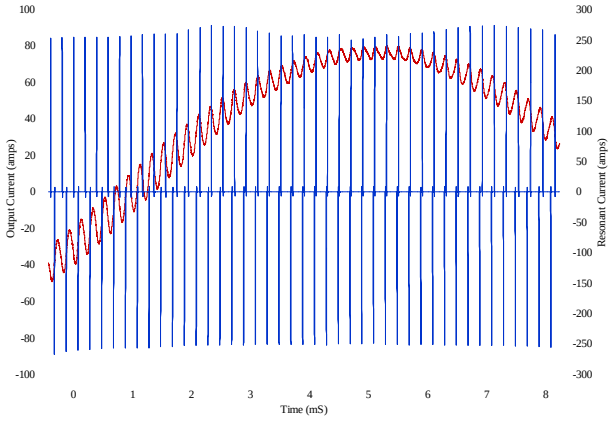

Figure 3. Fixed overlap time.

The next step in control algorithm improvement was to use the input DC bus voltage as a feedback sig-

nal. In this case the controller would read the DC bus voltage through a voltage transducer and calculate the required overlap time based on the known value of the resonant inductor. As the DC bus voltage increased, the controller automatically adjusted the overlap between phase and AC switch. Since no correction was being made for load current magnitude and direction, there was still significant unneeded resonant energy supplied at times during the switching cycle.

The most significant improvement in the control algorithm came with the development of the LMARC (Load Modulated Auxiliary Resonant Current) control software. The goal of the LMARC software was to provide the minimum amount of resonant energy to the circuit to allow a zero voltage transition to occur. This in turn produces the least amount of current stress to the main and auxiliary switches and improves overall inverter efficiency. LMARC works by feeding back the instantaneous three phase load currents to the ARCP controller. Given the interdependence of circuit characteristics, changes were made to the feedback control software in small incremental steps. Adequate safety margins (i.e. more resonant energy than what is theoretically needed) were maintained to insure zero voltage transitions in each of these steps.

The first step was to separate the resonant current requirements of the upper and lower main switches and control those overlap times individually. A consequence of the ARCP topology is that in order to guarantee proper operation, both the upper switch and the lower switch must be turned on for some period of time during each switching cycle. Therefore, two zero voltage transitions must occur during each switching cycle for each phase. The magnitude and direction of the instantaneous load current flowing through a main switch or diode can either be a help or a hindrance in these resonant transitions. The load current is always helping one of the transitions, meaning less resonant current is required from the auxiliary circuit. During the alternate switching event, when it is hindering, more resonant current is required from the auxiliary circuit. Therefore, the amount of time the auxiliary switch is left on must be individually set for each transition.

In this control strategy the output load current was first sampled three times and averaged prior to each switching event. Averaging was performed to minimize potential measurement errors stemming from electrical noise. With the resonant inductor value preprogrammed into the controller and the input bus voltage data known, the controller could calculate the required amount of overlap time for each switching event. The initial implementation of this control algorithm maintained a minimum overlap time for all switching events increasing only those which required a higher resonant current based on load current magnitude and direction. At light load, a viewed sequence of resonant pulses would appear to be of equal magnitude alternating in positive and negative directions similar to fixed overlap operation. When load current was increased, resonant current pulses began to grow in magnitude based on the load current. This increase was notable where switch transitions were made from a conducting diode to a transistor. This is because the resonant current must first displace the load current being supplied by the diode and then provide additional energy to cause the phase output voltage to swing to the opposite rail. Figure 4 shows the waveforms captured during the initial implementation of the LMARC control program. As can bee seen in this diagram there is a phase shift between the stream of resonant pulses and the actual load current. This was attributed to limitations in the original implementation of the control feedback loop. The ac-

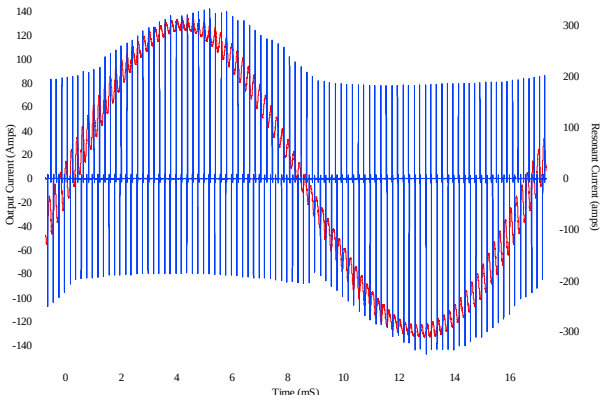

Figure 4. Load Modulated Auxiliary Resonant Current (LMARC) Control.

tual points in time when the load current samples were being taken and the sending of the calculated overlap times to the gate drives were too far apart. Improvements were made to the software program to allow the sampling times to be brought in closer in time to when the switching action was required to take place. Figure 5 shows the resonant pulse and load current waveforms after the software timing improvements were made. Note that the stream of pulses is much more closely aligned in phase with the load current.

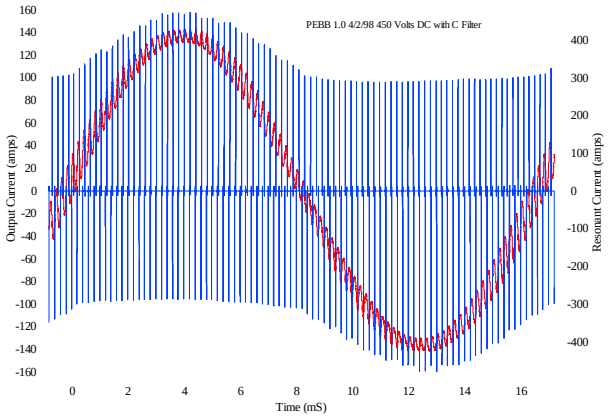

Figure 5. Improved LMARC

A further enhancement to the LMARC control program was to eliminate unneeded resonant pulses or to perform "pulse inhibit". When a high current transistor-to-diode switch transition is made, the current is in the proper direction to reduce the amount of auxiliary resonant current required. If it is above a predetermined threshold level, a resonant current pulse does not need to be generated. The high load current will actually force the phase output voltage to the opposite rail. As can be seen in Figure 6, the resonant pulses are eliminated when the load current is above 80 amperes.

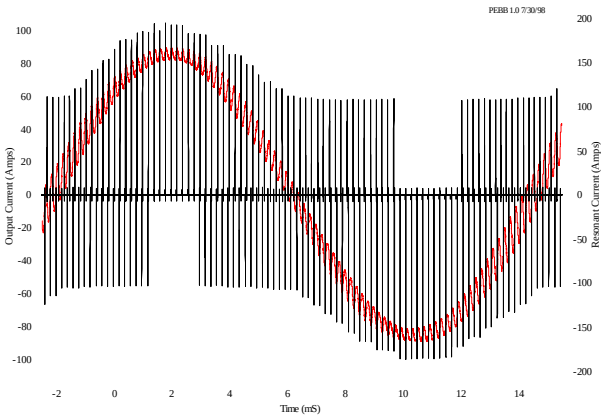

Figure 6. Pulse Inhibit

Improved Load Current Output Filter

At 5 kHz switching frequency there is still a significant peak to peak current ripple in the fundamental output current waveform. LMARC requires an accurate, and equally important, up to date sampling of the load current magnitude to determine the required overlap time for each resonant pulse generated. Because of these rapid current fluctuations the three average sampled data points could be off significantly from the actual current. This became more of an issue when pulse inhibit was invoked. As can be seen in Figure 6, the number of pulses dropped during the positive and negative half cycles of the load current waveform are unequal when in fact, they should have been equal. This unequal pulse dropping, caused by inaccuracies in instantaneous load current sensing, could lead to a midpoint bus voltage imbalance if not corrected. A shunt filter tuned to the 5kHz switching frequency was added across each of the load current transformers. This reduced the switching current peak to peak ripple to approximately 10% of its original value. To ensure that sufficient overlap time was generated the filtered current feedback signal current was added to a value equal to 0.6 times the peak to peak ripple current. Figure 7 shows the improvement in the resonant pulse generation as a result of adding the shunt filters.

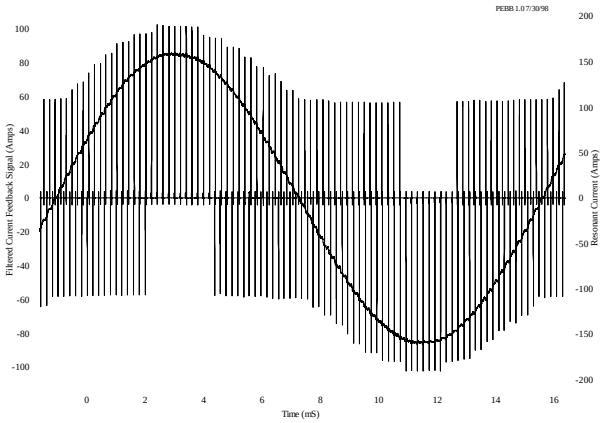

Figure 7. Pulse Inhibit with shunt filter.

Modified Pulse Inhibit

An even further reduction in resonant current losses was sought which led to the modified pulse inhibit. This modification tapers the resonant current pulses to nearly zero prior to reaching pulse inhibit (See Figure 8). Work is continuing in this area to determine what the optimum resonant current waveform should look like.

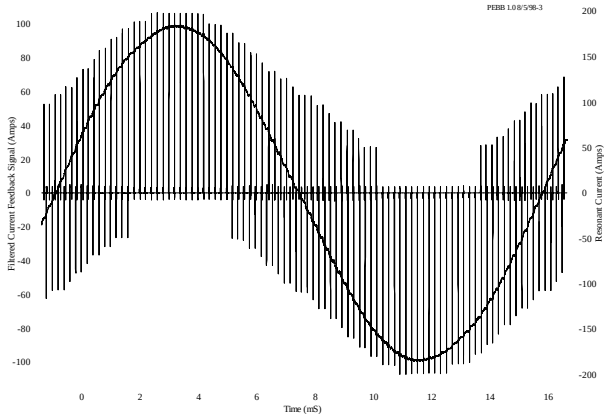

Figure 8. Modified Pulse Inhibit

Voltage Balance

Improvements in the control software have also been made with respect to three phase output voltage balance. Initial test runs had always yielded several volts of unbalance between the three phases. This was found to be attributable to two software operations. First, the software was modified to compensate for the differing overlap times for sequentially alternating positive and negative transitions. Second, the program was altered to compensate for the 1/3rd of a switching cycle between phases. A comparison of the output voltage balance before and after software implementation is presented in Table 1. Input DC bus voltage and output load were maintained at the same values for each run.

Phase A-B Voltage (Vac)	Phase B-C Voltage (Vac)	Phase C-A Voltage (Vac)	Phase Voltage Unbalance % (Worst case dev. /average)	Control Algorithm
137.4	134.4	137.4	1.47	Without Voltage Balance
136.6	136.4	136.6	0.10	With Voltage Balance

Table 1. Voltage Balance Before and After Software Implementation.

Bus Voltage Utilization

The line-to-line RMS voltage obtainable from a three phase PWM inverter is given as:

$$V_{L-L,\,RMS} = \frac{\sqrt{3} * m_a * V_D}{\sqrt{2}}$$

$$V_{L-L,\,RMS} \cong 0.612 * m_a * V_D$$

Where m_a is the amplitude modulation ratio and V_D is the DC bus voltage [2]. A common drawback of soft switching inverter topologies is the amount of time needed to perform the resonant switch cycle. This time cuts into the amount of duty cycle time available to synthesize the output waveform. Typically, for a hard switched inverter, one allows a few microseconds of "dead time" between the turning off of an upper switch and the turning on of a lower phase switch and vice versa during the other transition. This is done to prevent a shoot through condition from occurring where both an upper and lower

device are on simultaneously, shorting out the DC bus. This limits maximum duty cycle values to somewhere around 95-97%. In addition to the "dead time" found in hard switched inverters, soft switched inverters add resonant transition times which can push this maximum duty cycle value down significantly. An analysis of soft switching schemes reveals that some topologies fare better than others when it comes to how much time is lost due to resonant transitions. One of the reasons the ARCP inverter was chosen over other topologies was that its transition cycles were on the lower side of the spectrum compared to others [3]. Nevertheless, the NSWC ARCP had to deal with the trade off of maximizing DC bus utilization while producing high quality output waveforms through the use of high switching frequencies. At 5kHz switching frequency, the ARCP was able to operate at a duty cycle of 90% with conservative safety margins. It is estimated that a 95% duty cycle is achievable with the current hardware implementation.

Third Harmonic Voltage Injection

In order to get as much output voltage as possible from a given input voltage, the control algorithm was modified to include the technique known as third harmonic voltage injection. See reference [4] for an explanation of how this works. The net result of incorporating this into the control algorithm was a 15% increase in RMS voltage over the original algorithm.

Conclusions

This paper demonstrates the progression in software development for an ARCP inverter. The software is now available for full power testing of the Navy's laboratory model. Planned testing includes maximum power operation as well as efficiency measurements and harmonic distortion as a function of load current. Final testing will compare soft and hard switching utilizing the same hardware components with the exception of the AC switches and the connection of the resonant capacitors.

References

[1] R. W. DeDonker, "Resonant Pole Converters", EPE-93, Ch. 4, p 4-1 through 4-44, 1993

[2] Ned Mohan, Tore M. Undeland, William P. Robbins, *Power Electronics: Converters, Applications, and Design*, Second Edition, John Wiley and Sons, Inc., 1995

[3] Jeffrey Mayer, "Analysis of Zero-Current Switching Topologies and Strategies for the Power Electronic Building Block", Final Technical Report prepared under contract N00039-97-D-0042 for Naval Surface Warfare Center, February 1998

[4] John A. Houldsworth, Duncan A. Grant, "The Use of Harmonic Distortion to Increase the Output Voltage of a Three Phase PWM Inverter," IEEE Transactions on Industry Applications Vol. 1A –20. No. 5. Sept/Oct 1984, ppg 1224-1228